REMARKS

Claims 1-24 are pending. Claims 1-14 are allowed. Claims 15-16, 20-21, and 23-24 are rejected under 35 U.S.C. § 103(a). Claims 17-19 and 22 are objected to.

Claims 15-16 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Rao (U.S. Pat. No. 6,041,389). Claims 15-16 define a very specific structure of the present invention as shown at Figure 8 and described at page 9, line 21 through page 11, line 12. In particular, claims 15-16 recite "an address table (A0-Am) arranged to store a plurality of addresses and coupled to receive an external address (from bus 870); a data table (D0-Dm) coupled to the address table and arranged to store a first plurality of data words (CAM 602 includes a 32-word address table A0-Am and a corresponding 32-word data table D0-Dm, page 9, lines 22-23), each data word corresponding to a respective address in the address table; a nonvolatile memory circuit (Figure 7) arranged to store a second plurality of data words (6 Mbit FRAM array 710 is organized as 196,608 32-bit words, page 9, line 2) greater than the first plurality; and a data terminal coupled to the data table and to the nonvolatile memory circuit." (reference numerals added). The invention of claims 15-16 advantageously routes multiple memory accesses to a same memory address to data table 840 (Figure 8) rather than to the FRAM array 710 (Figure 7). This greatly reduces fatigue of the FRAM array.

Rao fails to teach or suggest these features or the corresponding advantages. Examiner admits that Rao fails to disclose an address table and a data table. (Office Action 7/19/05, page 2, paragraph 2). Examiner states "address buffer/latch 206 storing row address words from volatile content addressable memory CAM 207 and providing row address words to nonvolatile ferroelectric random access memory (FRAM) cell arrays 202." Applicant and Rao respectfully disagree. Referring to column 6, lines 25-35, Rao specifically teaches that CAM memory cells 207 are compared to bank select bits on bus 210. If they match, the CAM memory array 207 then enables address buffer/latch 206. Thus, CAM memory 207 **does not** provide row address words to anything.

Examiner applies his apparent misunderstanding of Rao to conclude "it would have been obviously included an address table and an data table as recited in claim 15." No, the CAM memory 207 of Rao compares bank select bits on bus 210 to CAM cells. Match line 211 enables address buffer/latch 206 if they match. If the CAM memory 207 is taken as the address table of claim 15, where is the data table? CAM memory 207 **does not** store data words as required by claim 15. Rao **does not** disclose "a data table coupled to the address table and arranged to store a first plurality of data words, each data word corresponding to a respective address in the address table" as required by claim 15. Since Rao **does not** disclose a data table, Rao also **does not** disclose "a data terminal coupled to the data table and to the nonvolatile memory circuit" as required by claim 15.

Rao discloses (Figure 2) a multibank memory (Bank 0 through Bank X) that may be configured for individual access or parallel access by writing a Bank Select address into each CAM array 207 at system initialization. (col. 6, lines 38-51). Examiner states "Input/output circuitry 213 obviously including address table to store addresses . . . data table to store data words . . . and providing all control signal and system clocks to control the system." (Office Action 4/1/05, page 4, paragraph 6). To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. Here, the limitations of claims 15-16 are simply not disclosed by Rao. There is no address table or corresponding data table. There is not even a reason to think there might be an address table or corresponding data table, since the invention of Rao is directed to a completely different purpose. Thus, applicant respectfully submits that claims 15-16 are patentable under 35 U.S.C. § 103(a) over Rao.

Claims 20-21 and 23-24 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Rao. Claims 20-21 and 23-24 define a very specific structure of the present invention as shown at Figures 6-8 and described at page 7, line 3 through page 11, line 12. In particular, claims 20-21 and 23-24 recite "a nonvolatile memory circuit (Figure 7) arranged to store a first data word (same as D0) at a first address (same as A0); a volatile memory circuit (D0-Dm) arranged to store the first data word (D0) and the first address (A0); a data bus (610 Figure 6) coupled to the processor and the volatile and nonvolatile memory circuits; and an address bus (608 Figure 7) coupled to the processor and the volatile and nonvolatile memory circuits." (reference numerals added). These features of the present invention are simply not disclosed by Rao. If data stored in memory array 202 of Rao (Figure 2) is taken as "a first data word" of claims 20-24, there is no corresponding volatile memory circuit to store the same "first data word" as required by claims 20-24. CAM array 207 only stores Bank Select address bits. (col. 6, lines 39-41). Thus, applicant respectfully submits that claims 20-21 and 23-24 are also patentable under 35 U.S.C. § 103(a) over Rao.

Rao fails to teach or suggest these features or the corresponding advantages. Examiner admits that Rao fails to disclose an address table and a data table. (Office Action 7/19/05, page 2, paragraph 2). Examiner states "address buffer/latch 206 storing row address words from volatile content addressable memory CAM 207 and providing row address words to nonvolatile ferroelectric random access memory (FRAM) cell arrays 202." Applicant and Rao respectfully disagree. Referring to column 6, lines 25-35, Rao specifically teaches that CAM memory cells 207 are compared to bank select bits on bus 210. If they match, the CAM memory array 207 then enables address buffer/latch 206. As previously explained, CAM memory 207 **does not** provide row address words to anything. If memory array 202 is taken as "a nonvolatile memory circuit arranged to store **a first data word at a first address**" Rao **does not** disclose "a volatile memory circuit arranged to store **the first data word and the first address**" as required by claims 20-21 and 23-24. Memory array 202 stores data. CAM array 207 stores bank select address bits. Therefore, both memories 202 and 207 could not possibly both store **the first data word at the first address** as required by claims 20-21 and 23-24.

Claims 20-21 and 23-24 further recite "a data bus coupled to the processor and the volatile and nonvolatile memory circuits." Referring to Figure 2, Rao discloses data bus 208 coupled to memory array 202 via column decode circuit 205 and sense amps 204. Rao **does not** disclose CAM array 207 is coupled to data bus 208. Match line 211 from CAM array 207 only enables address buffer/latch 206. (col. 6, lines 29-35). Match line 211 is not coupled to data bus 208. Thus, Rao **does not** disclose "a data bus coupled to the processor and the volatile and nonvolatile memory circuits" as required by claims 20-21 and 23-24.

Finally, claims 20-21 and 23-24 recite "an address bus coupled to the processor and the volatile and nonvolatile memory circuits." Referring to Figure 2, Rao discloses address bus 209 is coupled to memory circuit 202, 203, 205. Rao further discloses bank select bus 210 is coupled to CAM array 207. Rao **does not** disclose "an address bus coupled to the . . . volatile and nonvolatile memory circuits" as required by claims 20-21 and 23-24. For all the foregoing reasons, claims 20-21 and 23-24 are patentable under 35 U.S.C. § 103(a) over Rao.

In view of the foregoing, applicant respectfully requests reconsideration and allowance of claims 15-24 without further amendment. If the Examiner finds any issue that is unresolved, please call applicant's attorney by dialing the telephone number printed below.

Respectfully submitted,

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